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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,410	11/16/2001	Nigel G. Herron	X-915 US	3711

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EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/11/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/991,410	Applicant(s) HERRON ET AL.
	Examiner David Ton	Art Unit 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *IDS filed 01/16/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-26* is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-26 are presented for examination.

Claim Rejections - 35 USC ' 102

2. Claims 1-2 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Beebe et al. (Beebe) patent no. 6,021,513.

3. As to claim 1, Beebe teaches the invention as claimed, including a method for testing circuitry in an FPGA [see claim 6], comprising:

Configuring the FPGA for test including the FPGA forming an FPGA scan chain [see step (b) of claim 6] for simulating an external connection to an embedded device [programmable logic units of claim 6];

Receiving and conducting at least one device scan chain to the embedded device [see claim 17, step d(3)]; and

Performing test [see claim 18, step d(4-7)].

4. As to claim 2, Beebe teaches isolating the embedded device [see step d(7) of claim 18].

Claim Rejections - 35 USC ' 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3-18 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Beebe et al. (Beebe) patent no. 6,021,513, in view of Crouch et al. (Crouch) patent no. 5,592,493.

7. As to claims 3-4, Beebe does not teach transmitting test signal to a multiplexer for delivery to the embedded device.

Crouch teaches a scan chain architecture to route data through six functional units [see Fig. 1] including a test controller scan chain select 10 for demultiplexing the input data stream to one of the six units and an output multiplexer 24 to route data from one of the six units to the STDO pin [see col. 7 lines 5-25 and claim 1].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the teachings of Beebe to include the test controller taught by Crouch to form an interface for testing selected core device. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would improve test efficiency and effectiveness.

8. As to claim 5, Beebe teaches storing the test output signal in the scan chain [step d(5) of claim 18 (latching)].

9. As to claim 6, Beebe teaches receiving one device scan chain includes test output signals from the embedded device [see step d(6) of claim 18].

10. As to claims 7-8, Crouch teaches transmitting test data to an external tester [col.5 lines 50-68].

11. As to claim 9, Beebe teaches a method for testing an FPGA comprising configuring the FPGA for test as discussed in claim 1 above. However, Beebe does not teach transmitting a test signal to a multiplexer formed within a gasket to a device under test.

Crouch teaches a scan chain architecture to route data through six functional units [see Fig. 1] including a test controller scan chain select 10 for demultiplexing the input data stream to one of the six units and an output multiplexer 24 to route data from one of the six units to the STDO pin [see col. 7 lines 5-25 and claim 1].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the teachings of Beebe to include the test controller taught by Crouch to form an interface for testing selected core device. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would improve test efficiency and effectiveness.

12. As to claim 10, Crouch teaches the device under test is an embedded core device [devices 12-22 of Fig. 1].

13. As to claim 11, Crouch teaches the device under test is a fixed logic device formed within the gasket [see claims 1-2].

14. As to claim 12, Beebe teaches configuring the FPGA for test includes receiving an FPGA scan chain with test vectors [step 4(d) of claim 18].

15. As to claim 13, Crouch teaches receiving and conducting at least one device scan chain to the device under test [see claim 2].

16. As to claim 14, Beebe and Crouch teaches the invention substantially as discussed in claim 9 above. Furthermore, Beebe teaches transmitting the test signal to the FPGA fabric portion [the output boundary scan chain, see claim 18] and Crouch teaches transmitting the output test signal from the multiplexer to a partition scan chain [the vertical scan chain coupled between MUX 24 and the SDO pin which passes through all the functional blocks 12-22, see Fig. 1 and col. 7 lines 5-25].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the teachings of Beebe to include the test controller taught by Crouch to form an interface for testing selected core device by transmitting the test signal from the Crouch's multiplexer to Beebe's scan chain. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would improve test efficiency and effectiveness.

17. As to claims 15-18, they are similar to claims 10-13, therefore, they are rejected under the same rationale.

Allowable Subject Matter

18. Claims 19-26 are allowed.

Conclusion

19. The prior art of record and not relied upon is considered pertinent to applicant's disclosure.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached on Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DT

August 06, 2004

DAVID TON
PRIMARY EXAMINER